Remarks:

Reconsideration of the application is requested. It is noted that the application number on pages 2-7 of the Office action is incorrect.

Claims 1-20 remain in the application. Claim 5 has been amended. Claims 1-4 have been withdrawn from consideration at this time.

In item 5 on pages 3-5 of the above-mentioned Office action, claims 5-13, 17 and 19-20 have been rejected as being unpatentable over Iwai et al. (US Pat. No. 4,327,476) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 5 has been amended in an effort to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a metal-oxide-layer formed on said semiconductor substrate, said metal-oxide-layer containing molecules in the form of a metal-oxide-compound; and
>
> an oxidation inhibiting layer on said metal-oxide-layer.

The object of the invention of the instant application is to avoid a diffusion of oxygen from the metal oxide layer (3) into the electrode layer (5). If such a diffusion would occur, an additional oxide layer could be established by an oxidation of the electrode material caused by the diffused oxygen (see page 3, lines 14-22 of the specification). In order to prevent the formation of a parasitic electrode-oxide-layer, the oxidation inhibiting layer is provided on top of the metal oxide layer. It is, therefore, vital for the invention of the instant application that a metal oxide layer be present. The metal oxide layer is formed of molecules in the form of a metal-oxide-compound.

Iwai et al. disclose a method of manufacturing semiconductor devices. However, Iwai et al. do not disclose a metal-oxide-layer. The capacitive electrode structure shown in Iwai et al. (see Fig. 3J) includes a substrate 11, an insulating layer 17 and a polysilicon layer 16. Further, there is an insulating layer 18 and a gate electrode 20. A metal plug 25 contacts the gate electrode 20. Not a single layer or portion of a layer as shown in Fig. 3J is formed from a metal-oxide as defined above.

The Examiner has interpreted the word MOS as metal oxide layer (see middle of page 3 of the Office action). However, the meaning of the abbreviation MOS is not defined in Iwai et al.

When compared to well known textbooks, for example Itoh ("VLSI Memory Chip Design", page 199, Fig 4.5), a MOS capacitor includes a substrate, a silicon oxide layer formed on the substrate and a metal plate formed on the silicon layer. A metal-oxide-layer is not present. The abbreviation MOS stands for a layer stack including a separate metal layer, which includes metal atoms, and a separate insulation layer, which is an oxide layer, for example silicon oxide. Itoh does not contain a metal-oxide-layer which has molecules of a metal oxide compound.

Clearly, Iwai et al. do not show "a metal oxide layer formed on said semiconductor substrate, the metal oxide layer containing molecules in the form of a metal-oxide-compound; and an oxidation inhibiting layer on said metal oxide layer", as recited in claim 5 of the instant application.

Claim 5 is, therefore, believed to be patentable over the art and since claims 5-13, 17, and 19-20 are ultimately dependent on claim 5, they are believed to be patentable as well.

In item 6 on pages 5-6 of the above-mentioned Office action, claims 14-16 and 18 have been rejected as being unpatentable over Iwai et al. in view of Ackerman(US Pat. No. 5,547,706) under 35 U.S.C. § 103(a).

As discussed above, claim 5 is believed to be patentable over the art. Since claims 14-16 and 18 are ultimately dependent on claim 5, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 5-20 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

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Respectfully submitted,

For Applicants

YHC:cgm

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Marked-Up Version of the Amended Claims:

Claim 5(amended). A capacitive electrode structure, comprising:

a semiconductor substrate;

a [metal oxide layer] metal-oxide-layer formed on said semiconductor substrate, said metal-oxide-layer containing molecules in the form of a metal-oxide-compound;

an oxidation inhibiting layer on said metal-oxide-layer; and

an electrode on said oxidation inhibiting layer.